Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**1 16**

**A**

**123**

**15**

**14**

**13**

**12**

**11**

**10**

**2**

**3**

**4**

**5**

**6**

**7**

**8 9**

**MASK**

**REF**

**.055”**

**.100”**

**PAD FUNCTION:**

1. **1A**
2. **1B**
3. **1 CLR**
4. **1Q**
5. **2Q**
6. **2C ext**
7. **2R ext/C ext**
8. **GND**
9. **2A**
10. **2B**
11. **2 CLR**
12. **2Q**
13. **1Q**
14. **1C ext**
15. **1R ext/C ext**
16. **VCC**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: 123 A**

**APPROVED BY: DK DIE SIZE .055” X .100” DATE: 2/10/22**

**MFG: TEXAS INSTRUMENTS THICKNESS .024” P/N: 54123**

**DG 10.1.2**

#### Rev B, 7/1